Ex) Build acet of half-adder using:-

ⓐ NOR gate only.

ⓑ NAND gate only.

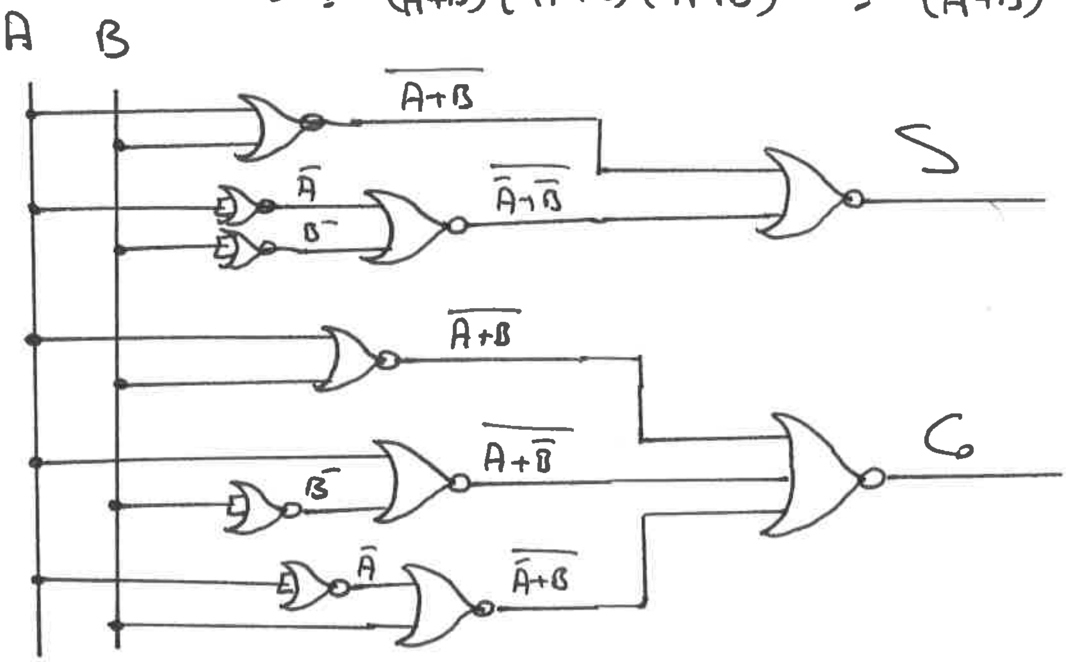
ⓐ using NOR gate

$$S = (A+B)(\bar{A}+\bar{B})$$

$$S = \overline{\overline{(A+B)(\bar{A}+\bar{B})}} = \overline{\overline{(A+B)} + \overline{(\bar{A}+\bar{B})}}$$

$$C_o = \overline{\overline{(A+B)(\bar{A}+B)(A+\bar{B})}}$$

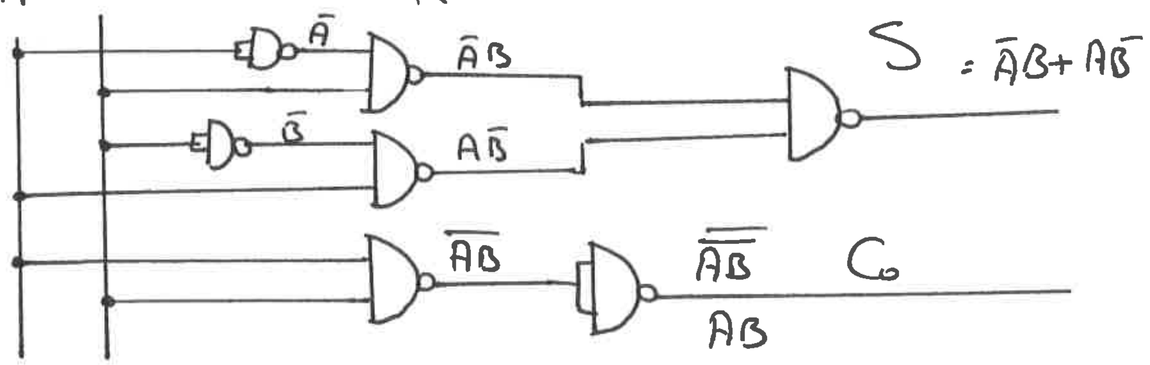
$$C_o = \overline{\overline{(A+B)(\bar{A}+B)(A+\bar{B})}} = \overline{\overline{(A+B)} + \overline{(A+\bar{B})} + \overline{(\bar{A}+B)}}$$



ⓑ Using NAND gate

$$S = \bar{A}B + A\bar{B} = \overline{\overline{\bar{A}B + A\bar{B}}} = \overline{\overline{A\bar{B}} \cdot \overline{\bar{A}B}}$$

A B $\quad C_o = AB = \overline{\overline{AB}}$



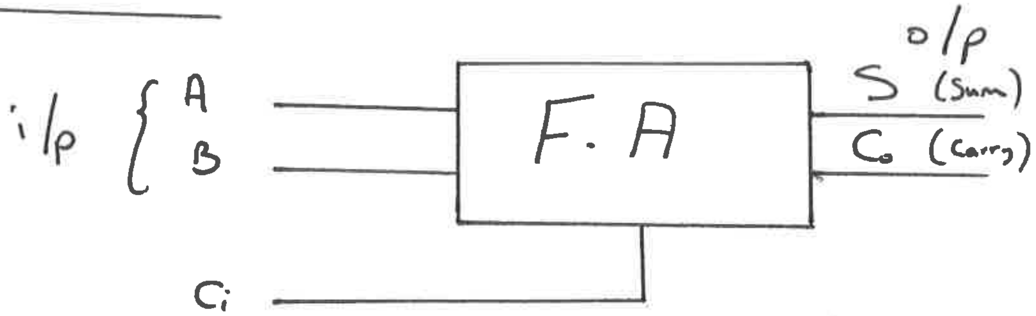
Full Adders

A Full-adder is a Combinational Circuit that performs the arithmetic Sum of three input bit. It consists of three inputs and two outputs.

Truth table :-

i/p			o/p	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Block Diagram



"Block diagram of Full-Adder (F.A)".

From truth table :-

$$S = \Sigma\ 1, 2, 4, 7$$

$$S = m_1 + m_2 + m_4 + m_7$$

$$= \bar{A}\bar{B}C_i + \bar{A}B\overline{C_i} + A\bar{B}\overline{C_i} + ABC_i$$

$$= C_i(\underline{AB + \bar{A}\bar{B}}) + \overline{C_i}(A\bar{B} + \bar{A}B)$$

$$= C_i(A \oplus B) + \overline{C_i}(A \oplus B)$$

$$\therefore S = A \oplus B \oplus C$$

$$C_o = \Sigma\ 3, 5, 6, 7$$

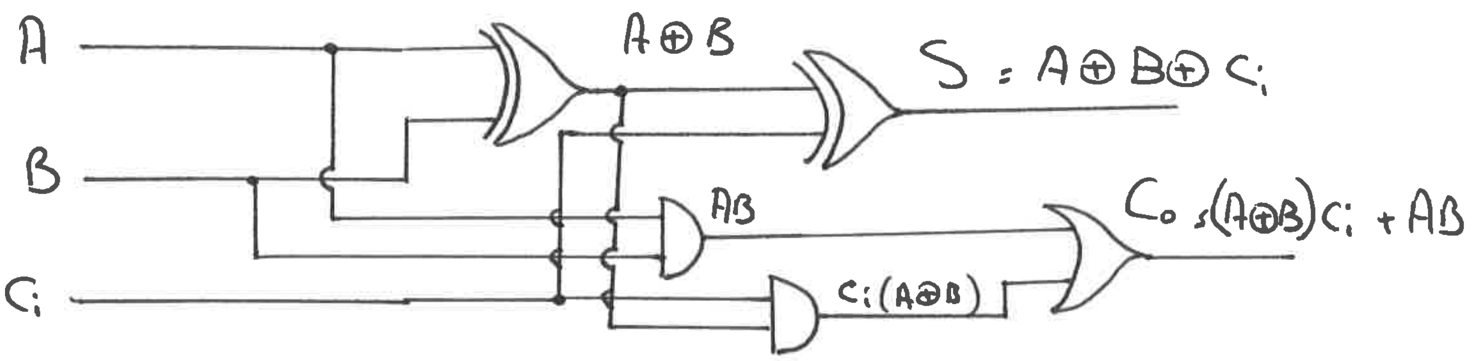
$$C_o = m_3 + m_5 + m_6 + m_7$$

$$= \bar{A}BC_i + A\bar{B}C_i + AB\overline{C_i} + ABC_i$$

$$= C_i(A\bar{B} + \bar{A}B) + AB$$

$$\therefore C_o = C_i(A \oplus B) + AB$$

Logic cct



$$S = A \oplus B \oplus C$$

$$C_o = C_i(A \oplus B) + AB$$

by Using K-Map

A \ BC_i	00	01	11	10
0		1		1
1	1		1	

S

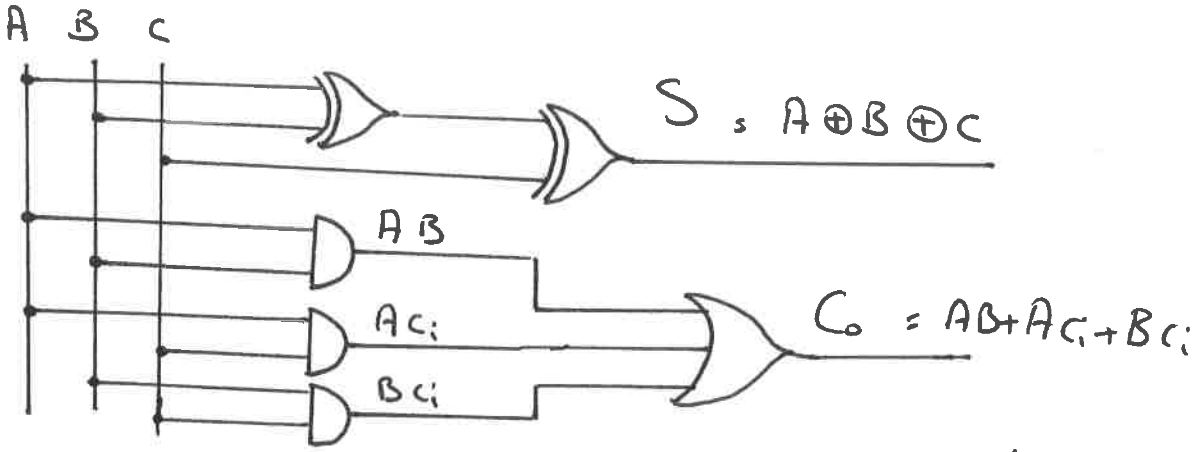
A \ BC_i	00	01	11	10
0			1	
1		1	1	1

C_o

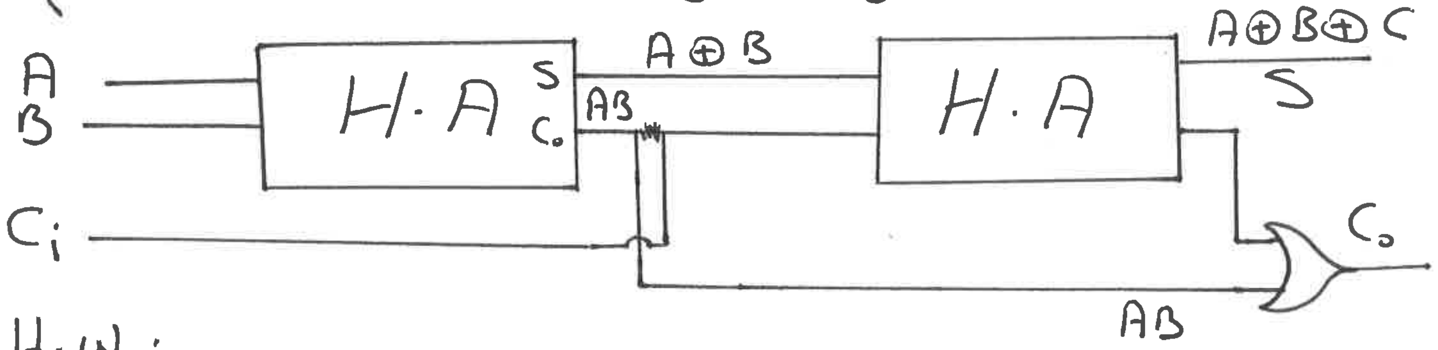
$$S = \bar{A}\bar{B}C_i + \bar{A}B\bar{C_i} + ABC_i + A\bar{B}\bar{C_i}$$

$$= A \oplus B \oplus C$$

$$C_o = AB + AC_i + BC_i$$



Ex) Build a Full-Adder by using two half-adder?



H.W :-

Ex) Build F.A by using NAND gate only?

Ex) Build F.A by using NOR gate only?

Ex) Design a Logic cct to provide an o/p of Logic (1) where every any two of three inputs are Logic (1)?

Subtractors :-

A subtractors is a combinational circuit that subtract bits and produces their difference.

There are two types of subtractors

① Half-Subtractor (H.S).

② Full-Subtractor (F.S).

① Half-Subtractor (H.S)

A half-subtractor is a combinational circuit that subtract two bits and produces their difference.

The truth table

i/p		o/p	
A	B	D	Bo
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

where :-

D = Difference.

Bo = Barrow.

From truth table

$D = \Sigma\ 1, 2$

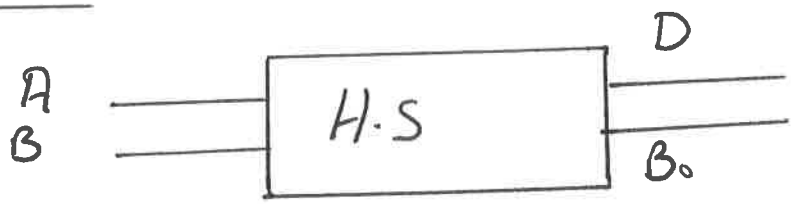
$= A\bar{B} + \bar{A}B$

$D = A \oplus B$

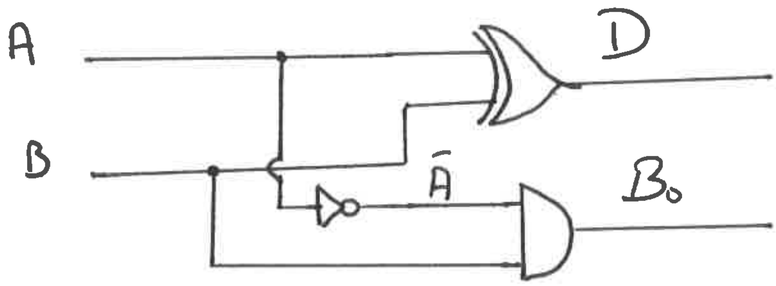
$B_o = \Sigma\ 1$

$B_o = \bar{A}B$

The Block Diagram



The Logic cct



Ex) Build H.S by using NAND gate only ? \ H.W
Ex) " " " " NOR " " ?

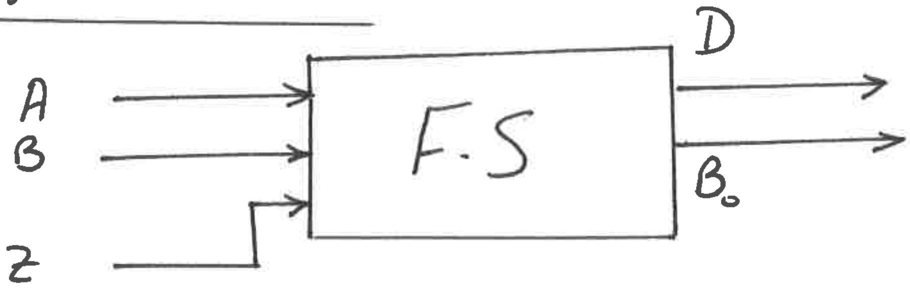
Full-Subtracter:-

A Full-Subtractor is a Combinational Circuit that Performs a Subtraction between two bits taking into account that a (1) may have been borrowed by a Lower

Significant stages.

This cct has three input and two outputs.

Block-Diagram of (F.S)



The truth table:-

i/p			o/p	
A	B	Z	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

From truth table

$$D = \Sigma\, 1, 2, 4, 7$$

$$B_o = \Sigma\, 1, 2, 3, 7$$

$$D = \bar{A}\bar{B}Z + \bar{A}B\bar{Z} + A\bar{B}\bar{Z} + ABZ$$

$$= Z(\bar{A}\bar{B} + AB) + \bar{Z}(A\bar{B} + \bar{A}B)$$

$$= Z(\overline{A \oplus B}) + \bar{Z}(A \oplus B)$$

$$D = A \oplus B \oplus Z$$

$$B_o = \bar{A}\bar{B}Z + \bar{A}B\bar{Z} + \bar{A}BZ + ABZ$$

$$= Z(\bar{A}\bar{B} + AB) + \bar{A}B(Z + \bar{Z})$$

$$= Z(\bar{A}\bar{B} + AB) + \bar{A}B$$

$$= Z(\overline{A \oplus B}) + \bar{A}B$$

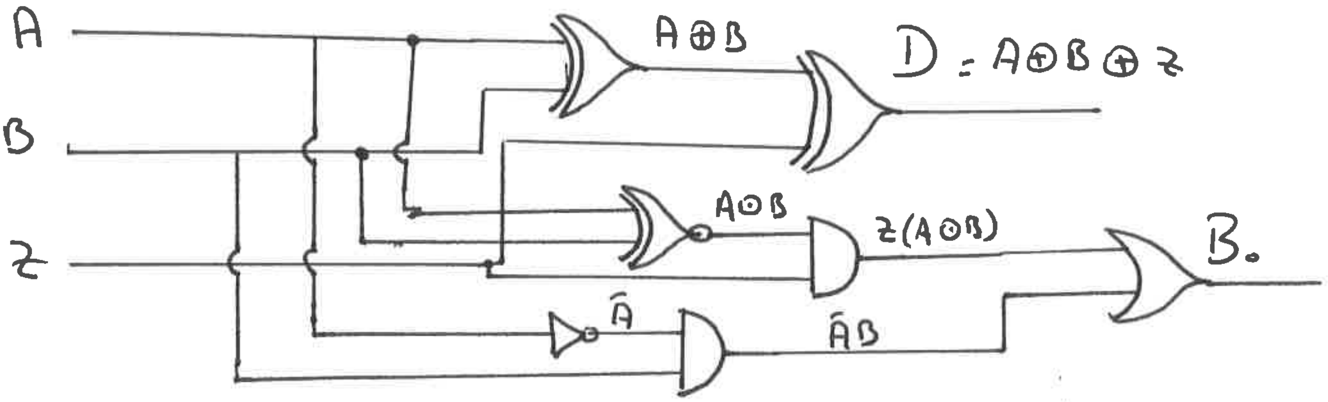
$$B_o = Z(A \odot B) + \bar{A}B$$

By using K-Map

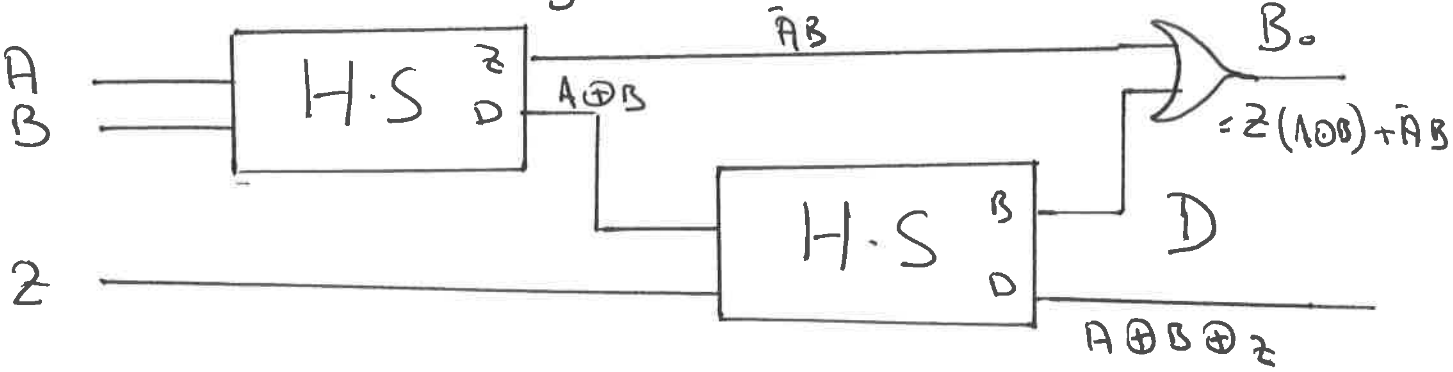
A \ BZ	00	01	11	10
0		1	1	1
1			1	

$$B_o = \bar{A}B + \bar{A}Z + BZ$$

The Logic cct



Ex) Implement a F.S by means of H.S ?



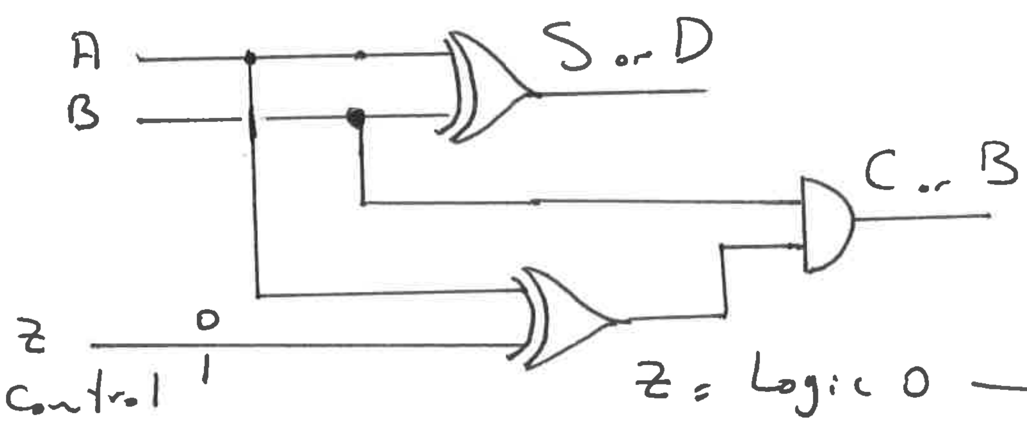
In H/A $\quad S = A \oplus B$

$\qquad\qquad C = AB$

In H/S $\quad D = A \oplus B$

$\qquad\qquad B = \bar{A}B$

We can implment a Logic cct to (ADD or Substract), by using controller as fellow:-



Z = Logic 0 $\longrightarrow$ H/A

Z = Logic 1 $\longrightarrow$ H/S

Ex) By mean's of Block diagram of H/A and two OR gates. Design a Logic cct that convert a decimal digit from the 8 4 -2 -1 code to BCD code?

i/p 8 A	4 B	-2 C	-1 D	o/p (BCD) w	x	y	z
0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	0	1	0	0	1	1
0	1	0	0	0	1	0	0
1	0	1	1	0	1	0	1
1	0	1	0	0	1	1	0
1	0	0	1	0	1	1	1
1	0	0	0	1	0	0	0
1	1	1	1	1	0	0	1

$w = \Sigma\ 8, 15$

$x = \Sigma\ 4, 11, 10, 9$

$y = \Sigma\ 6, 5, 10, 9$

$z = \Sigma\ 7, 5, 11, 9, 15$

$z = D$

don't care $= \Sigma\ 1, 2, 3, 12, 13, 14$

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$		X	X	X
$\bar{A}B$				
AB	X	X	1	X
$A\bar{B}$	1			

$$W = AB + A\bar{C}\bar{D}$$

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$		X	X	X
$\bar{A}B$	1			
AB	X	X		X
$A\bar{B}$		1	1	1

$$X = B\bar{C}\bar{D} + \bar{B}D + \bar{B}C$$

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$		X	X	X
$\bar{A}B$		1		1
AB	X	X		X
$A\bar{B}$		1		1

$$y = \bar{C}D + C\bar{D}$$

$$y = C \oplus D$$

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$		X	X	X
$\bar{A}B$		1	1	
AB	X	X	1	X
$A\bar{B}$		1	1	

$$Z = D$$